REMARKS

Applicants are amending their claims in order to further clarify the definition of various aspects of the present invention. Specifically, Applicants have amended claim 18, the sole independent claim in the application, to recite that the step of removing the IC element and securing the IC element is performed with a temporary securing pin "that is disposed over the IC element holding part". Claim 18 has also been amended at lines 16 and 17 to recite "the" IC element and "the" IC elements transport mechanism.

Initially, it is respectfully requested that the present amendments be entered, notwithstanding the Finality of the Office Action mailed January 11, 2010. In this regard, it is respectfully submitted that amendments to line 16 of claim 18 are clearly appropriate, in light of the objection to claim 18 in Item 3 on page 2 of the Office Action mailed January 11, 2010, and the required correction in connection therewith. Furthermore, it is respectfully submitted that amendment to line 25 of claim 18 does not raise any new issues, in light of, for example, previously considered claim 36; and clearly this amendment of claim 18 does not raise any issue of new matter, noting, for example, Fig. 3(e) of Applicants' original disclosure, especially as described in the paragraph bridging pages 21 and 22 of Applicants' specification. Note also Fig. 4(f), and the description in connection therewith in the sole full paragraph on page 25 of Applicants' specification. Noting the new reference applied by the Examiner in the Office Action mailed January 11, 2010, and new arguments made by the Examiner in this Office Action mailed January 11, 2010, it is respectfully submitted that the present amendments are timely; and by further clarifying differences between the present invention and the teachings of the applied

references, it is respectfully submitted that the present amendments materially limit issues remaining in connection with the above-identified application, and, at the very least, present the claims in better form for appeal.

In view of the foregoing, it is respectfully submitted that Applicants have made the necessary showing under 37 CFR 1.116(b)(3), and, accordingly, entry of the present amendments is clearly proper.

The objection to claim 18, due to "informalities" alleged by the Examiner in Item 3 on page 2 of the Office Action mailed January 11, 2010, is noted. Applicants have amended claim 18, in lines 16 and 17, to recite "the" IC element and "the" IC elements transport mechanism, complying with the suggestion by the Examiner in this Item 3. In view of this amendment to claim 18, it is respectfully submitted that the objection thereto has been overcome, and that the required "appropriate correction" has been made.

Applicants respectfully submit that all of the claims presented for consideration by the Examiner patentably distinguish over the teachings of the references applied by the Examiner in rejecting claims in the Office Action mailed January 11, 2010, that is, the teachings of the U.S. patent documents to Usami, et al., Patent No. 7,036,741, to Yamakawa, Patent No. 6,479,777, to McMahon, et al., Patent No. 5,751,068, to Green, et al., Patent Application Publication No. 2003/0136503, and to Moskowitz, et al., Patent No. 5,528,222, under the provisions of 35 USC 103.

It is respectfully submitted that these references as applied by the Examiner would have neither disclosed nor would have suggested such a manufacturing method for an electronic device as in the present claims, including, inter alia, a step

of positionally aligning connection surfaces of the IC elements and either one of the circuit layers while continuously supplying the IC elements individually into an IC elements transport mechanism, wherein the continuously supplying the IC elements includes, inter alia, individually holding the IC element in an IC holding part, of an IC elements transport mechanism, which is formed as a notch shape; delivering the IC element to a position over an anisotropic conductive adhesive layer disposed on one of the circuit layers; and removing the IC element from the IC element holding part and securing the IC element held by the IC element holding part at any of the circuit layers with a temporary securing pin that is disposed over the IC element holding part when the IC element is over the anisotropic conductive adhesive layer. See claim 18.

It is emphasized that according to the present invention the IC element is delivered by running the IC element holding part to the position over an anisotropic conductive adhesive layer that is disposed on the first circuit layer or the second circuit layer, and removing the IC element from the IC element holding part and securing the IC element at any of the circuit layers with a temporary securing pin that is disposed over the IC element holding part, when the IC element is over the anisotropic conductive adhesive layer. Thus, according to the present invention, using the IC elements transport mechanism having the IC element holding part, and the temporary securing pin disposed over the IC element holding part, as in the present claims, the IC element is separately transferred by the IC elements transport mechanism to the position over the anisotropic conductive adhesive layer that is disposed on the first or second circuit layer, e.g., positionally aligned with respect to the connection surfaces of the IC elements, and further at that position the IC

element is removed from the IC element holding part by the temporary securing pin, in a simple and quick procedure that achieves accurate positioning, and secured over the anisotropic conductive adhesive layer on the first or second circuit layer. For example, the IC element can be secured on the anisotropic conductive adhesive layer by the temporary securing pin disposed over the IC element holding part, by simply pressing downward, at the securing position, the temporary securing pin, without transporting movement of the temporary securing pin and IC element to the position where the IC element is secured. Accordingly, operation of removing the IC element from the IC element holding part, and securing such IC element on the circuit layer, can be performed in a substantially small amount of time, and in a simple manner, as compared, for example, with the prior art. For example, the operation time for transporting, securing and connecting can be reduced to not more than about one second.

Moreover, by providing a step of positionally aligning the connection surfaces of the IC elements and either one of the circuit layers while continuously supplying the IC elements individually into an IC elements transport mechanism, as in claim 18, a plurality of individual IC elements can be directly and simultaneously transported, positionally aligned and secured individually, so that securing on tapes or extracting from tapes, such as tape automated bonding, is not necessary, whereby effective productivity and low costs are realized.

By performing the step of securing the IC elements utilizing the temporary securing pin disposed over the IC element holding part, the held IC elements can be extracted easily and efficiently, and immediately secured on the lower circuit layers.

According to the present invention, utilizing features as discussed previously, positional alignment is performed while continuously supplying the IC elements individually into the IC elements transport mechanism, so that, e.g., the securing can be done with a desired accuracy when the IC elements are separated, and securing with desired accuracy can be achieved even where the IC elements are very thin, for example, a thickness of less than 0.5 mm. The presently claimed process can easily transport a plurality of minute, thin and separated IC elements, positionally align them individually, and remove the IC elements from the transport mechanism and secure the elements on a circuit layer, so that effective productivity and low costs are realized.

Moreover, by simply pushing the IC elements from above by the temporary securing pin disposed over the IC element holding part, the IC elements can be removed and secured on the circuit layer. The circuit layer after securing IC elements has the configuration that a plurality of IC elements can be secured at predetermined intervals, and handling of the formed structure, and the following steps, can be performed in a single step. Therefore the present invention significantly shortens operating time, realizes effective productivity and provides lower cost.

Furthermore, it is respectfully submitted that these applied references would have neither disclosed nor would have suggested such a manufacturing method as in the present claims, having features as discussed previously in connection with claim 18, and, additionally, wherein the step of continuously supplying the IC elements includes a step of individually holding an IC element in an IC element

holding part of a transport mechanism, which is a disc shaped IC elements transport mechanism (see claim 20; note also claim 36).

In addition, it is respectfully submitted that the teachings of these applied references would have neither disclosed nor would have suggested such manufacturing method for an electronic device as in the present claims, having features as discussed previously in connection with claim 18, and, additionally, wherein the temporary securing pin only removes the IC element from the IC element holding part and secures the IC element at any of the circuit layers (see claim 25); and/or wherein the transport mechanism has the disc shape with notches as discussed previously, and wherein the temporary securing pin removes the IC element from the notches and secures the IC element on the anisotropic conductive adhesive layer (which, as set forth in claim 18, is under the IC element) (see claim 36).

According to aspects of the present invention, a simple processing can be used to transport the IC elements to an appropriate position, and, through use the temporary securing pin disposed over the IC element holding part, to remove the IC element and secure the IC element at a circuit layer.

In addition, it is respectfully submitted that these applied references would have neither disclosed nor would have suggested such a manufacturing method as in the present claims, having features as discussed previously in connection with claim 18, and, additionally, wherein the step of continuously supplying the IC elements includes a step of aligning the IC elements by action of an IC elements alignment/supply mechanism to facilitate individually holding the IC element in the holding part (note claims 22-24), in particular, wherein the IC elements

alignment/supply mechanism is a line feeder (see claim 23) or is a high frequency alignment feeder (see claim 24).

Moreover, it is respectfully submitted that the teachings of these applied references would have neither disclosed nor would have suggested such a manufacturing method as in the present claims, having features as discussed previously in connection with claim 18, and, additionally, having further features as in the remaining dependent claims, including (but not limited to) wherein the electrical connection of an electrode and at least one of the circuit layers is made via the anisotropic conductive adhesive layer (see claim 25); and/or wherein the method further includes connecting, at once, the electrodes of the IC elements and at least one layer from among the first and second circuit layers, with the step of connecting being performed after the step of positionally aligning the connection surfaces (see claim 26), in particular, wherein the electrode of the IC elements and the at least one layer from among the first and second circuit layers are connected by thermal compression (see claim 27), with gaps between the first and second circuit layers being sealed by the thermal compression (see claim 28); and/or wherein the method further includes a step of cutting a continuum of the plurality of IC elements into individual pieces, with the step of cutting being performed after the connecting step (see claim 29); and/or wherein a conductive layer is formed on the surface of at least one from among the first and second circuit layers (see claim 30); and/or wherein the first and second circuit layers include aluminum (see claim 31); and/or wherein a base substrate material supports at least one of the first and second circuit layers, the base substrate material being a material as in claims 32 and 33; and/or thickness of the anisotropic conductive adhesive layers, as in claim 34.

The present invention is directed to a method of manufacturing an electronic device, illustrated by (but not limited to) a noncontact type individual identification device having IC elements.

In recent years, individual identification systems that employ radio frequency identification tags have been considered; such systems include an external antenna attached to IC elements, which enables communication to be performed over several meters. One type of such system is a TCP (Tape Carrier Package) inlet, employing a tape automated bonding method in which IC elements having all external electrodes formed on the same surface thereof are mounted, each individually, on a tape carrier formed of a polyimide substrate.

As described in the first full paragraph on page 3 of Applicants' specification, other proposed inlet structures include IC elements in which the external electrodes of the IC elements are formed individually on both of a pair of opposite surfaces of the IC element. The IC elements in this proposed structure have, respectively, two external electrodes formed individually on the surfaces of the IC elements, and are furnished with an excitation slit type dipole antenna, the external electrodes formed individually on each of the surfaces of the IC elements being disposed between the legs of an antenna to manufacture a sandwich antenna construction.

However, various problems arise in connection with previously proposed inlet structures and methods of manufacture thereof, as described on pages 4 and 5 of Applicants' specification. Thus, it is still desired to provide a manufacturing method for manufacturing a semiconductor device, which can be utilized in an identification system, which can manufacture the device at low cost and with superior productivity, and wherein the device has satisfactory communication properties.

Against this background, Applicants achieve the foregoing objectives by the presently claimed manufacturing method, including, inter alia, wherein connection surfaces of IC elements and circuit layers are positionally aligned while continuously supplying the IC elements individually into an IC elements transport mechanism, with this step of continuously supplying the IC elements including (i) individually holding the IC element in an IC element holding part of the IC elements transport mechanism having not less than one IC element holding part which is formed as a notch shape, (ii) the IC element thus held is delivered by running the IC element holding part of the transport mechanism to a position over an anisotropic conductive adhesive layer that is disposed on a circuit layer, and (iii) the IC element is removed from the IC element holding part, and the IC element held by this holding part is secured at a circuit layer, with a temporary securing pin which is disposed over the IC element holding part, when the IC element is over the anisotropic conductive adhesive layer. Through such processing, relatively simple movement of the temporary securing pin enables securing of the IC element to the circuit layers, with movement of the IC elements transport mechanism moving the IC element to a position over the anisotropic conductive adhesive layer, the IC element to be removed and secured by the temporary securing pin. Such relatively simple movement for transporting and securing an IC element to a circuit layer not only simplifies the apparatus used and the necessary movement, but also reduces operation time for transporting and securing the IC element to the anisotropic conductive adhesive layer.

That is, according to the present invention, when, e.g., a small and thin IC element is supplied individually, the IC element can be easily transported, separately positionally aligned and secured, and there exists no need to secure and remove IC

elements from a tape. Moreover, because the IC element transport mechanism with the IC element holding part transports the IC elements separately to the position over the anisotropic conductive adhesive layer, traveling distance by the temporary securing pin, and operating time thereof, can be reduced significantly, advantageously achieving improved productivity and reduced costs.

Moreover, by continuously supplying the IC elements individually into an IC elements transport mechanism as in the present claims, in particular, into a notch at the periphery of a disc shaped transport mechanism, a plurality of IC elements up to a maximum number equivalent to the number of, e.g., notches, can be delivered, even when the delivered IC elements are arranged individually on the second circuit layer and the antenna circuits, so that superior productivity can be realized in comparison to the case where the IC elements are held by suction using a vacuum suction device or the like, and delivered and arranged one by one. As increased productivity is realized, available operating time per inlet device is reduced. Note the first full paragraph on page 16 of Applicants' specification.

By forming the connecting structure (that is, the first through third connecting parts, particularly the second and third connecting parts) spanning the slit, high precision positional alignment of the external electrode on that surface of the IC elements that is on the side in contact with the antenna circuit, with the excitation slit on the antenna circuit, is not necessary, thus reducing costs associated with manufacturing equipment and facilitating high-speed delivery of the IC elements. See page 16, lines 13-18, of Applicants' specification.

By providing electrical connections via an anisotropic conductive adhesive layer, as in all of the present claims, it is not necessary to have a surface coating

over the antenna circuits, and there is no need to use a highly heat resistant base substrate, making it possible to use an inexpensive base material and antenna circuit, thereby enabling cost reductions. Note the paragraph bridging pages 16 and 17 of Applicants' specification.

In particular, as the IC elements are accommodated individually, e.g., in notches in the IC elements transport mechanism, with a plurality of notches arranged circumferentially around, e.g., the outside of a disc-shaped transport mechanism, a maximum number of IC elements equivalent to the number of notches can be simultaneously delivered, providing improvement in the productivity. Note the last full paragraph on page 18 of Applicants' specification.

Usami, et al. discloses a technique effectively applied to a structure of a wireless IC chip used to identify an object in a non-contact manner, an IC tag for wirelessly sending an identification number, a transponder, or the like. The device has electrodes formed on front and rear surfaces of an IC chip for wirelessly transmitting/receiving data, first and second conductors being connected respectively to the electrodes. The first and second conductors include a slit, and the first and second conductors are connected to each other. See column 3, lines 58-64; note also column 3, lines 50-57; and column 4, lines 11-26. Note also column 5, lines 52-56, describing that the conductors are attached to each other with anisotropic conductive adhesive. Note column 10, lines 54-58; and column 11, lines 25-30. Note, further, column 17, lines 46-50.

It is respectfully submitted that Usami, et al. would have neither disclosed nor would have suggested such procedure as in the present claims, including, <u>inter alia</u>, positionally aligning the connection surfaces of the IC elements and either one of the

circuit layers while continuously supplying the IC elements individually into an IC elements transport mechanism, or further definition of continuously supplying the IC elements including the delivering of the IC element, and removing and securing the IC element, as in claim 18.

The Examiner contends on page 4, lines 4-7, of the Office Action mailed January 11, 2010, that Usami, et al. discloses the step of positionally aligning, referring to Fig. 15A of this reference, together with column 18, lines 33-42. Such contention by the Examiner is respectfully traversed. It is respectfully submitted that Fig. 15A of Usami, et al. discloses positional alignment between a tape that mounts IC chips and another tape that has circuit layers, by use of the sprockets formed on each tape. It is respectfully submitted that this disclosure in Usami, et al., as relied upon by the Examiner, does not teach, nor would have suggested, positional alignment between individual IC elements themselves, and circuit layers.

Moreover, it is respectfully submitted that the positional alignment using sprockets, as in Usami, et al., requires tape automated bonding, and it is respectfully submitted that Usami, et al. would have neither disclosed nor would have suggested, and in view of requirements thereof would have taught away from, handling separated IC elements, as achieved by the present invention.

Furthermore, it is respectfully submitted that Usami, et al. would have neither taught nor would have suggested other features of the present invention as in claim 18, including, inter alia, delivering the IC element held by the IC element holding part to the position over the anisotropic conductive adhesive layer over the pertinent circuit layer, and removing and securing the IC element held by the IC element holding part, with a temporary securing pin disposed over the IC element

holding part, when the IC element is over the anisotropic conductive adhesive layer. It is respectfully submitted that Usami, et al. discloses use of a vacuum absorber that attaches IC chips on the second conductor by airflow, referring to Fig. 7 and a corresponding description in column 12, lines 23-26 of Usami, et al. A configuration that the held IC elements are secured on circuit layers with a temporary securing pin disposed as in the present claims, when the IC element is located as recited in the present claims, would have neither been disclosed nor suggested by Usami, et al. By using airflow to attach IC chips on the second conductor, as in Usami, et al., accurate positional alignment is not obtainable. Moreover, use of a vacuum absorber to suck and transport the large number of IC chips simultaneously using a plurality of sucking sets requires a complex facility and large-scale plant investments, so that low-cost production becomes difficult. Such problems are avoided by the present invention, using the temporary securing pin disposed as in the present claims.

It is respectfully submitted that the teachings of the secondary references as applied by the Examiner would not have rectified the deficiencies of Usami, et al., such that the presently claimed invention as a whole would have been obvious to one of ordinary skill in the art.

Yamakawa discloses a conveying apparatus that conveys electronic parts such as chip-type capacitors and resistors, and a method of use thereof. This patent discloses use of a conveying table which is rotationally driven in a constant direction, the table including a plurality of concave storage slots formed with identical pitches on the entire outer-peripheral section of the table. These slots store chip-type electronic parts, each slot having a bottom surface, two radial side surfaces, and an

inner-circumferential side surface. Further, an air hole is provided, having one end open on the inner-circumferential side surface and the other end communicating with a negative air pressure source generating negative suction air pressure that sucks the electronic part onto the inner-circumferential side surface of the concave storage slot. The electronic part is vacuum-suctioned by negative air pressure provided through the air hole onto the concave storage slot. See column 2, lines 1-19; note also column 2, lines 52-60.

Yamakawa pushes the IC chips in the tangential direction, and is unable to positionally align so as to place the IC chips at a desired position on the circuit layers with accuracy. Even combining the teachings of Usami, et al. and Yamakawa, such combined teachings would have neither disclosed nor would have suggested the presently claimed manufacturing method as in all of the present claims, including, inter alia, the step of positionally aligning the connection surfaces of the IC elements and either one of the circuit layers while continuously supplying the IC elements individually into an IC element transport mechanism, or delivering to the positions over the specified anisotropic conductive adhesive layer, or the removing and securing with the temporary securing pin disposed over the IC element holding part, when the IC element is over the adhesive layer.

It is emphasized that the combined teachings of Usami, et al. and of Yamakawa would have neither taught nor would have suggested other features of the present invention, including, inter alia, removing the IC element and securing the IC element held by the IC element holding part at any of the circuit layers with a temporary securing pin disposed over the IC element holding part. It is respectfully submitted that the apparatus set forth in Yamakawa, and use of such apparatus in

the process of Yamakawa, supplies IC chips using airflow. It is respectfully submitted that such technique requires relatively thick IC chips, for example, the thickness of the IC chip is required to be not less than 0.5 mm in Yamakawa. It is respectfully submitted that Yamakawa is not applicable to IC chips that have a thickness less than 0.5 mm, such as chips for RFID tags. Thus, it is respectfully submitted that the teachings of Yamakawa, either alone or together with the teachings of Usami, et al., would have neither disclosed nor would have suggested the presently claimed invention, including such feature of use of the temporary securing pin disposed as in the present claims, and advantages thereof in that IC chips having a small thickness, of, e.g., 0.15 mm, with a relatively small height and width or, e.g., 0.4 mm, can be processed and precisely positioned, among other advantages.

McMahon, et al. discloses a technique for transferring solder forms to chips, chip packages or printed circuit boards. The method as described transfers solder forms to electronic components having conductive pads, and includes (a) positioning and temporarily placing a plurality of sets of the solder forms on a roll of tape; (b) aligning a first set of the solder forms to the conductive pads of a first one of the electronic components; (c) releasing the first set of the solder forms from the roll of tape; and (d) contacting the first set of the solder forms to the conductive pads of the first one of the electronic components. Note column 2, lines 23-31; see also column 2, lines 31-33. See also column 1, lines 53-59. As applied by the Examiner, note Fig. 7 and the description in connection therewith in column 6, lines 46-56. Described therein is a mechanical arm which places electronic components 77 such as chip packages, chips or PCBs on the bottom side of a rotatable table 73. When

an electronic component and a tape portion having solder forms are rotated to a position 76, the electronic component is pressed against the tape portion to attach the tape portion with the solder forms to the electronic component; and, after the attachment, the electronic component with the tape portion and the solder forms may be left on rotatable table 73 or on rotatable tray 72 to be picked up by another mechanical arm.

Even taking the teachings of McMahon, et al. together with the teachings of Usami, et al. and of Yamakawa, it is respectfully submitted that the combined teachings of these references would have neither disclosed nor would have suggested such manufacturing method as in the present claims, including, inter alia, wherein the step of continuously supplying the IC elements includes, inter alia, a step of removing the IC element from the IC element holding part and securing the IC element held by the IC element holding part using a temporary securing pin that is disposed over the IC element holding part, when the IC element is over the anisotropic conductive adhesive layer.

Contentions by the Examiner in connection with the teachings of McMahon, et al., on pages 6 and 7 of the Office Action mailed January 11, 2010, are noted. In particular, to be noted is the contention by the Examiner in the last two lines on page 6 of the Office Action mailed January 11, 2010, that “it is obvious that the chips are pressed using some sort of a pin as is known in the art”. Such contention by the Examiner is respectfully traversed. Contrary to this contention by the Examiner it is respectfully submitted that there is no indication or suggestion that the electronic components disposed at the bottom side of the rotating table, as expressly disclosed in McMahan, et al., are removed with a temporary securing pin as recited in the

present claims, much less wherein such temporary securing pin is disposed over the IC element holding part, as in the present claims.

It is respectfully suggested that in McMahon, et al., it may be appropriate that the electronic components disposed at the bottom side of the upper rotating table, and the tape having solder balls disposed at the lower rotating table, are secured by pressing each other through sandwiching between the upper and lower rotating tables. In that case, due to the non-homogenous pressure at the contacting portion between the upper and lower rotating tables, the distortion of the rotating tables may arise, and precision for securing the electronic components may be deteriorated. Further, the electronic components can not be densely disposed on the rotating table, because the contacting portion between the rotating tables only accepts the electronic component being secured. Consequently, the rotating table needs to be substantially rotated for pressing one electronic component against the solder balls, requiring increased operating time and thereby lowering productivity.

In contrast, according to the present invention the IC elements are secured to the circuit layer using the temporary securing pin disposed over the IC element holding part; and the rotating table does not receive pressure for securing the IC elements, so that precision for securing can be maintained because no distortion of the rotating table should arise. In addition, the present invention can densely dispose the electronic components on the rotating table, thereby decreasing the necessary rotation angle of the rotating table between IC elements and thereby reducing operating time for each step.

Furthermore, it is emphasized that McMahon, et al., at column 6, lines 46-49, discloses a mechanical arm to place electronic components 77 such as chip

packages, chips or PCBs on the <u>bottom side</u> of rotating table 73; this means that the electronic components are disposed <u>at the bottom side of the rotating table</u>. Based on this description, it is respectfully submitted that it would be structurally difficult to remove the electronic component, disposed at the bottom side of the rotating table, and to secure on the circuit layer disposed at the lower side of the rotating table, using a temporary securing pin disposed <u>over</u> the rotating table. In contrast, the present invention utilizes a temporary securing pin <u>disposed over the IC holding part</u>, and by use of such pin pushing the IC elements <u>from above</u> the IC elements can be removed and secured on the circuit layer, further decreasing operating time.

Applicants also respectfully traverse the contention by the Examiner on page 6 of the Office Action mailed January 11, 2010, that McMahon, et al., discloses a step of delivering an IC element “to a position over an anisotropic conductive adhesive layer”. It is respectfully submitted that the adhesive of McMahon, et al., is utilized for securing the solder balls to the tape (see column 5, lines 22-28, of McMahon, et al.), <u>not</u> for securing the IC elements on the circuit layer as in the present invention. <u>In addition</u>, it is respectfully submitted that only solder flux and optically sensitive adhesive are exemplified in McMahon, et al., (note, e.g., column 5, lines 22-28), and it is respectfully submitted that <u>anisotropic conductive adhesive layer</u> is <u>not</u> disclosed nor would have been suggested by the teachings of McMahon, et al.

In contrast, it is respectfully submitted that the present invention allows securing the IC element to the anisotropic conductive adhesive layer on the first circuit layer or the second circuit layer, utilizing the temporary securing pin that is disposed over the IC element holding part, when the IC element is over the

anisotropic conductive adhesive layer, which allows securing the IC element at relatively low temperatures and in a reduced time, and also suppresses occurrence of voids, thereby shortening the operating time and increasing reliability of the electrical connection.

As can be seen in the all of the foregoing, it is respectfully submitted that even taking the teachings of McMahon, et al. together with the teachings of Usami, et al. and of Yamakawa, such combined teachings would have neither disclosed nor would have suggested the manufacturing method of claim 18, including, inter alia, securing the IC element held by the IC element holding part at any of the circuit layer with a temporary securing pin that is disposed over the IC element holding part, when the IC element is over the anisotropic conductive adhesive layer, and advantages achieved thereby; and/or other features of the present invention as discussed in the foregoing, and advantages achieved thereby.

It is respectfully submitted that the additional secondary references applied by the Examiner in the Office Action mailed January 11, 2010, on pages 10-12 of the Office Action mailed January 11, 2010 would not have rectified the deficiencies of the combined teachings of Usami, et al., Yamakawa, et al. and McMahon, et al., such that the presently claimed invention as a whole would have been obvious to one of ordinary skill in the art.

In connection with claims 27, 28 and 31, Moskowitz, et al. discloses a radio frequency circuit and memory in a thin flexible package, used as a radio frequency tag. The radio frequency tag includes a semiconductor circuit that has logic, memory and radio frequency circuits, the semiconductor being mounted on a substrate and being capable of receiving a RF signal through an antenna that is electrically

connected to the semiconductor through connections on the semiconductor. The elements of the package are placed adjacent to one another, that is, they are not stacked. See column 3, lines 9-20. Note also from column 3, line 65, through column 4, line 10, disclosing, inter alia, the antenna of the tag, manufactured as an integral part of the substrate. See column 5, lines 53-59 of this patent.

Even assuming, arguendo, that the teachings of Moskowitz, et al. were properly combinable with the teachings of Usami, et al. of Yamakawa, and of McMahon, et al., such combined teachings would have neither disclosed nor would have suggested the presently claimed invention, including, inter alia, delivering the IC element held by the transport mechanism to the recited location, and removing and securing the IC element with the temporary securing pin, disposed over the IC element holding part when the IC element is at the recited location, and advantages of the present invention due thereto.

In connection with claims 32 and 33, Green, et al. discloses methods of manufacturing radio frequency identification tags and labels, which include providing an RFID web stock having a plurality of recesses, each of the recesses containing an RFID chip, with a second web being provided having antennas spaced thereon. The RFID web stock is divided (severed, or separated) into a plurality of sections, each of the sections including one or more of the RFID chips. The pitch of the RFID sections is indexed from a high pitch density on the RFID web stock, to a relatively low pitch density on an RFID inlay stock. The sections are attached to a plurality of antennas in an automatic continuous process, so that each of the RFID chips is joined to one of the antennas to form an RFID inlay stock. Note paragraph [0021] on page 2 of Green, et al.; see also paragraph [0022] on page 2 thereof.

Even assuming, arguendo, that the teachings of Green, et al. were properly combinable with the teachings of Usami, et al., Yamakawa, McMahon, et al. and Moskowitz, et al., such combined teachings would have neither disclosed nor would have suggested the presently claimed invention, including, inter alia, the step of delivering the IC element held by the transport mechanism to the recited location, and the step of removing and securing using a temporary securing pin, disposed over the IC element holding part when the IC element is at the specified location, as in all of the present claims, and advantages thereof; and/or other features of the present invention as discussed previously, and advantages thereof.

In view of the foregoing comments and amendments, entry of the present amendments, and reconsideration and allowance of all claims presently pending in the above-identified application, are respectfully requested.

To the extent necessary, Applicants hereby petition for an extension of time under 37 CFR 1.136. Kindly charge any shortage of fees due in connection with the filing of this paper, including any extension of time fees, to the Deposit Account of Antonelli, Terry, Stout & Kraus, LLP, Account No. 01-2135 (case 1204.46401X00), and please credit any overpayments to such Deposit Account.

Respectfully submitted,

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